LISTING OF CLAIMS

1. (Currently Amended) A computer based test bench generator for verifying an integrated circuit memory model ~~circuits specified by models in a Hardware Description Language~~, comprising:

a repository storing an identification of memory models catalogued according to memory type, number of ports and synchronous/asynchronous functional operation ~~a general set of self-checking tests applicable to integrated circuits~~;

means for entering behavior data of a memory ~~an integrated circuit~~ model under test, the behavior data comprising an identification of ports in the memory model under test and a description for each such port of port cycles and port behavior;

means for entering configuration data of the memory ~~integrated circuit~~ model under test;

means for automatically generating test benches ~~in said Hardware Description Language~~, said means being configured to make a selection ~~and setup~~ of suitable types of tests based on a match between the entered configuration data of the memory model under test and the catalogued memory models from said repository and further setup by executing a software-based test case file generation algorithm which generates specific test vectors for each of the selected test types that are unique to the memory model under test according to the ~~specified integrated circuit model,~~ configuration and behavior data.

2. (Canceled).

3. (Currently Amended) The test bench generator of claim 1, wherein said test benches are ~~general set of tests is~~ specified in said Hardware Description Language.

4. (Currently Amended) The test bench generator of claim 3 ~~2~~, wherein said Hardware Description Language is VERILOG.

5. (Currently Amended) The test bench generator of claim 1 ~~[[3]]~~, wherein said behavior data is specified in a proprietary language.

6. (Currently Amended) The test bench generator of claim 1 ~~[[3]]~~, wherein said configuration data is input to said means for generating ~~generator~~ through a command line.

7. (Original) The test bench generator of claim 1 ~~[[3]]~~, wherein said selection of tests is based on conditional statements.

8. (Currently Amended) A method for verifying integrated circuits specified by integrated circuit memory models ~~in a Hardware Description Language~~, comprising the steps of:

storing an identification of memory models catalogued according to memory type, number of ports and synchronous/asynchronous functional operation ~~a general set of self-checking tests applicable to integrated circuits~~ in a repository;

entering behavior data of a memory ~~an integrated circuit~~ model under test, the behavior data comprising an identification of ports in the memory model under test and a description for each such port of port cycles and port behavior;

entering configuration data of the memory ~~integrated circuit~~ model under test;

selecting of ~~and setting up~~ suitable types of tests based on a match between the entered configuration data of the memory model under test and the catalogued memory models from said repository; and

setting-up by executing a software-based test case file generation algorithm which generates specific test vectors for each of the selected test types that are unique to the memory model under test according to the ~~specified integrated circuit model,~~ configuration and behavior data, so as to generate test benches ~~in said Hardware Description Language~~.

9. (Canceled).

10. (Currently Amended) The method according to claim 8, wherein said test benches are ~~general set of tests is~~ specified in said Hardware Description Language.

11. (Currently Amended) The method according to claim 8 ~~10~~, wherein said Hardware Description Language is VERILOG.

12. (Currently Amended) The method according to claim 8 ~~11~~, wherein said behavior data is specified in a proprietary language.

13. (Currently Amended) The method according to claim 8 ~~11~~, wherein said configuration data is input ~~to said generator~~ through a command line.

14. (Currently Amended) The method according to claim 8 ~~11~~, wherein said selection of tests is based on conditional statements.

15. (Currently Amended) A test bench generator for integrated circuit designs, comprising:

a repository which stores functional and structural characteristic data for integrated circuit models;

a processing functionality which receives an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model, the processing functionality operating to:

process the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; ~~and~~

compare the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model; and

execute a software-based test case file generation algorithm which generates specific test vectors for each of the identified applicable tests that are unique to the configured integrated circuit model in accordance with received model data.

16. (Currently Amended) The generator of claim 15 wherein the specific test vectors comprise ~~processing functionality further processes the identified tests which are applicable to produce~~ a set of self-checking test benches for the specific integrated circuit model.

17. (Original) The generator of claim 16 wherein the self-checking test benches are Verilog test benches.

18. (Original) The generator of claim 16 wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

19. (Original) The generator of claim 15 wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language.

20. (Original) The generator of claim 19 wherein the hardware description language is a Verilog language.

21. (Original) The generator of claim 15 further including a simulator functionality which applies the identified applicable tests against the configured integrated circuit model.

22. (Currently Amended) A test bench generation method for integrated circuit designs, comprising:

storing functional and structural characteristic data for integrated circuit models;

receiving an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model;

processing the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; ~~and~~

comparing the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model; and

executing a software-based test case file generation algorithm which generates specific test vectors for each of the identified applicable tests that are unique to the configured integrated circuit model in accordance with received model data.

23. (Currently Amended) The method of claim 22 wherein the test vectors are ~~further including processing the identified tests which are applicable to produce~~ a set of self-checking test benches for the specific integrated circuit model.

24. (Original) The method of claim 23 wherein the self-checking test benches are Verilog test benches.

25. (Original) The method of claim 23 wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

26. (Original) The method of claim 22 wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language.

27. (Original) The method of claim 26 wherein the hardware description language is a Verilog language.

28. (Original) The method of claim 22 further including applying the identified applicable tests against the configured integrated circuit model to simulate operation.